

What Is Claimed Is:

1 1. A method of forming an integrated circuit transistor,
2 comprising:
3 proving a semiconductor substrate with a gate structure
4 formed thereon;
5 forming at least one dielectric layer overlying the
6 semiconductor substrate, wherein the at least one
7 dielectric layer comprises at least one first portion
8 along at least one sidewall of the gate structure,
9 and at least one second portion outside the gate
10 structure along the surface of the semiconductor
11 substrate;
12 forming at least one first doped region in the
13 semiconductor substrate laterally adjacent to the at
14 least one first portion of the at least one dielectric
15 layer, wherein the at least one second portion of the
16 at least one dielectric layer remains overlying the
17 at least one first doped region;

18 forming a sidewall spacer overlying the at least one
19 dielectric layer along the at least one sidewall of
20 the gate structure; and
21 forming at least one second doped region in the
22 semiconductor substrate laterally adjacent to the
23 sidewall spacer.

1 2. The method of forming an integrated circuit
2 transistor of claim 1, wherein a thickness of the at least one
3 dielectric layer ranges from about 10 Angstroms to about 350
4 Angstroms.

1 3. The method of forming an integrated circuit
2 transistor of claim 1, further comprising a step of removing
3 exposed regions of the at least one dielectric layer before the
4 formation of the at least one second doped region.

1 4. The method of forming an integrated circuit
2 transistor of claim 1, wherein the formation of the at least one
3 dielectric layer is a blanket deposition of silicon oxide,
4 silicon oxynitride, alternating layers of silicon oxide and
5 silicon nitride, or combinations thereof.

1 5. The method of forming an integrated circuit
2 transistor of claim 1, wherein the formation of the at least one
3 dielectric layer is a blanket deposition by a chemical vapor
4 deposition (CVD) process using tetraethylorthosilicate (TEOS) .

1 6. The method of forming an integrated circuit
2 transistor of claim 1, wherein the sidewall spacer is silicon
3 oxide, silicon oxynitride, alternating layers of silicon oxide
4 and silicon nitride, or combinations thereof.

1 7. The method of forming an integrated circuit
2 transistor of claim 1, wherein the sidewall spacer is formed
3 using a blanket deposition process and a dry etch process.

1 8. The method of forming an integrated circuit
2 transistor of claim 1, wherein the at least one first doped
3 region is formed using an ion implantation process and an
4 annealing process.

1 9. The method of forming an integrated circuit
2 transistor of claim 8, wherein after the annealing process, the
3 at least one dielectric layer becomes a densified material which

4 exhibits an etch rate less than about 200 Angstroms/minute in
5 a 100:1 HF solution.

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1 10. A method of forming a semiconductor device,
2 comprising:
3 proving a semiconductor substrate with a gate structure
4 formed thereon;
5 blanket depositing at least one first dielectric layer
6 overlying the semiconductor substrate without
7 performing an etch process on the at least one first
8 dielectric layer;
9 wherein, the at least one first dielectric layer
10 comprises at least one first portion along at
11 least one sidewall of the gate structure;
12 wherein, the at least one first dielectric layer
13 comprises at least one second portion outside
14 the gate structure along the surface of the
15 semiconductor substrate; and
16 performing a first ion implantation process to form at
17 least one first doped region in the semiconductor
18 substrate laterally adjacent to the at least one
19 first portion of the at least one first dielectric

11. The method of forming a semiconductor device of claim
10, further comprising performing an annealing process to
activate ions of the at least one first doped region, wherein
the at least one first dielectric layer becomes a densified
material with an etch rate less than about 200 Angstroms/minute
in a 100:1 HF solution.

1 12. The method of forming a semiconductor device of claim
2 10, wherein a thickness of the at least one first dielectric
3 layer ranges from about 10 Angstroms to about 350 Angstroms.

1 13. The method of forming a semiconductor device of claim
2 10, wherein the at least one first dielectric layer is silicon
3 oxide, silicon oxynitride, alternating layers of silicon oxide
4 and silicon nitride, or combinations thereof.

1 14. The method of forming a semiconductor device of claim
2 10, further comprising:

3 depositing at least one second dielectric layer overlying
4 the at least one first dielectric layer;
5 etching the at least one second dielectric layer to form
6 at least one sidewall spacer along the at least one
7 sidewall of the gate structure; and
8 performing a second ion implantation process to form at
9 least one second doped region in the semiconductor
10 substrate laterally adjacent to the at least one
11 sidewall spacer.

1 15. The method of forming a semiconductor device of claim
2 10, wherein the at least one second dielectric layer is silicon
3 oxide, silicon oxynitride, alternating layers of silicon oxide
4 and silicon nitride, or combinations thereof.

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1 16. An integrated circuit transistor, comprising:
2 a semiconductor substrate having a gate structure;
3 at least one dielectric layer overlying the semiconductor
4 substrate, wherein the at least one dielectric layer
5 comprises at least one first portion along at least
6 one sidewall of the gate structure;
7 at least one first doped region in the semiconductor
8 substrate laterally adjacent to the at least one
9 first portion of the at least one dielectric layer;
10 a sidewall spacer overlying the at least one dielectric
11 layer along the at least one sidewall of the gate
12 structure; and
13 at least one second doped region formed in the
14 semiconductor substrate laterally adjacent to the
15 sidewall spacer;
16 wherein, the at least one dielectric layer is a densified
17 material with an etch rate less than about 200
18 Angstroms/minute in a 100:1 HF solution.

1 17. The integrated circuit transistor of claim 16,
2 wherein the at least one dielectric layer comprises at least one
3 second portion which covers the at least one first doped region.

1 18. The integrated circuit transistor of claim 16,
2 wherein the at least one dielectric layer is an L-shaped spacer
3 extending from the at least one sidewall of the gate structure
4 to the at least one first doped region.

1 19. The integrated circuit transistor of claim 16,
2 wherein a thickness of the at least one dielectric layer ranges
3 from about 10 Angstroms to about 350 Angstroms.

1 20. The integrated circuit transistor of claim 16,
2 wherein the at least one dielectric layer is silicon oxide,
3 silicon oxynitride, alternating layers of silicon oxide and
4 silicon nitride, or combinations thereof.

1 21. The integrated circuit transistor of claim 16,
2 wherein the at least one dielectric layer is a TEOS oxide layer.

1 22. The integrated circuit transistor of claim 16,
2 wherein the sidewall spacer is silicon oxide, silicon

3 oxynitride, alternating layers of silicon oxide and silicon
4 nitride, or combinations thereof.

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